What is Claimed is:

[c1] A method for performing parasitic extraction for a component having a plurality of ports comprising:

calculating a minimum output impedance for each of said ports;

estimating a maximum parasitic impedance for each of said ports;

determining an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports; and

extracting actual parasitic impedance values from ports where said maximum parasitic impedance exceeds said minimum output impedance by more than a predetermined amount.

[c2] The method of claim 1, wherein said step of calculating of said minimum output impedance includes tracing resistances within each net in said component from a supply along a least resistive path and adding resistances of resistors along said path.

[c3] The method of claim 1, wherein said step of calculating of said minimum output impedance includes calculating minimum capacitances within each net in said component, considering all bias conditions.

[c4] The method of claim 1, wherein said estimating of said maximum parasitic impedance is based on area and perimeter values of all nets in said component.

[c5] The method of claim 1, wherein said estimating of said maximum parasitic impedance is based on a geometry of nets in said component.

[c6] The method of claim 5, wherein said geometry comprise a summation of area and perimeter values of all said nets in said component.

[c7] The method of claim 1, wherein said estimating of said maximum parasitic impedance comprises calculating a resistance of a total length of wiring having an average wire width within an associated net within said component.

[c8] A method for performing parasitic extraction for a component having a plurality of ports comprising:

calculating a minimum output impedance for each of said ports;

estimating a maximum parasitic impedance for each of said ports;
determining an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports;
extracting actual parasitic impedance values from ports where said maximum parasitic impedance exceeds said minimum output impedance by more than a predetermined amount; and
using said estimated maximum parasitic impedance as said actual parasitic impedance for ports where said maximum parasitic impedance does not exceed said minimum output impedance by more than said predetermined amount.

[c9] The method of claim 8, wherein said step of calculating of said minimum output impedance includes tracing resistances within each net in said component from a supply along a least resistive path and adding resistances of resistors along said path.

[c10] The method of claim 8, wherein said step of calculating of said minimum output impedance includes calculating minimum capacitances within each net in said component, considering all bias conditions.

[c11] The method of claim 8, wherein said estimating of said maximum parasitic impedance is based on area and perimeter values of all nets in said component.

[c12] The method of claim 8, wherein said estimating of said maximum parasitic impedance is based on a geometry of nets in said component.

[c13] The method of claim 12, wherein said geometry comprise a summation of area and perimeter values of all said nets in said component.

[c14] The method of claim 8, wherein said estimating of said maximum parasitic impedance comprises calculating a resistance of a total length of wiring having an average wire width within an associated net within said component.

[c15] A system for performing parasitic extraction for a component having a plurality of ports comprising:

a calculator adapted to calculate a minimum output impedance for each

of said ports;

an estimator adapted to estimate a maximum parasitic impedance for each of said ports;

a comparator adapted to determine an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports; and

a selector adapted to extract actual parasitic impedance values from ports where said maximum parasitic impedance exceeds said minimum output impedance by more than a predetermined amount.

[c16] The system of claim 15, wherein calculator is further adapted to trace resistances within each net in said component from a supply along a least resistive path and add resistances of resistors along said path.

[c17] The system of claim 15, wherein said calculator is further adapted to calculate minimum capacitances within each net in said component, considering all bias conditions.

[c18] The system of claim 15, wherein said estimator bases said estimate of said maximum parasitic impedance on area and perimeter values of all nets in said component.

[c19] The system of claim 15, wherein said estimator bases said estimate of said maximum parasitic impedance on a geometry of nets in said component.

[c20] The system of claim 19, wherein said geometry comprise a summation of area and perimeter values of all said nets in said component.

[c21] A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine to perform a method for performing parasitic extraction for a component having a plurality of ports, said method comprising:

calculating a minimum output impedance for each of said ports;

estimating a maximum parasitic impedance for each of said ports;

determining an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports; and

extracting actual parasitic impedance values from ports where said maximum parasitic impedance exceeds said minimum output impedance by more than a predetermined amount.

[c22] The program storage device of claim 21, wherein said step of calculating of said minimum output impedance includes tracing resistances within each net in said component from a supply along a least resistive path and adding resistances of resistors along said path.

[c23] The program storage device of claim 21, wherein said step of calculating of said minimum output impedance includes calculating minimum capacitances within each net in said component, considering all bias conditions.

[c24] The program storage device of claim 21, wherein said estimating of said maximum parasitic impedance is based on area and perimeter values of all nets in said component.

[c25] The program storage device of claim 21, wherein said estimating of said maximum parasitic impedance is based on a geometry of nets in said component.

[c26] The program storage device of claim 25, wherein said geometry comprise a summation of area and perimeter values of all said nets in said component.

[c27] The program storage device of claim 21, wherein said estimating of said maximum parasitic impedance comprises calculating a resistance of a total length of wiring having an average wire width within an associated net within said component.